REMARKS

The comments of the applicant below are each preceded by related comments of the examiner (in small, bold type).

> **Claims 1-3,5,7-8, 10-11, 13-14, 16, 18-19, 21-22, 24-26, 39-40, 42-44, and 46-49 are rejected under 35 U.S.C. 102(e) as being anticipated by Qureshi et al. (US PG Publication 2004/0030856 A1), hereinafter Qureshi.**
>
> **As for claims 1,13, and 47, Qureshi teaches a method comprising:**
> **from at least two types of endian conversion each of which can be performed on a portion of data (page) stored within a memory system, determining a type (two types of conversion may be performed on the data by remapping the most significant and least significant bits (i.e. big-to-little, or little-to-big) - paragraphs 0004 and 0005, all lines. The determination for swapping occurs via the indicator stored in the endian selection register which is based on the determination the OS type) — see also Fig. 6 (step 607 discloses little endian conversion, and step 609 discloses big endian conversion - paragraphs 0022 and 0023, all lines); and**
> **writing an entry to a memory management table based on the determining (based on the determination of what type of conversion can be performed based on the OS type, the endian selection register is written to designate which type of swapping is required - paragraphs 0022 and 0023, all lines).**

Claim 1 has been amended to recite determining a type "from at least two types of endian conversion, including a first type which can be performed on a portion of data stored within a memory system and a second type which can be performed on the same portion of data...." As the examiner noted, *Qureshi* describes that a portion of data that can undergo either big-to-little endian conversion or little-to-big endian conversion, depending on whether the portion of data is big endian or little endian. [*See* para. 0023 ("If the OS is little endian, then the least significant bit (LSB) is re-mapped to the lowest memory address.... Otherwise, the memory is assumed to be big endian and the most significant bit (MSB) is re-mapped to the lowest memory address...."); *see also* Fig. 6]. A portion of data that is big-endian would always undergo a big-to-little conversion, and a portion of data that is little-endian would always undergo a little-to-big conversion. However, both types of endian conversion (big-to-little and little-to-big) would not be performed on the same portion of data. Therefore, *Qureshi* does not disclose and would not have suggested determining a type "from at least two types of endian conversion, including a

first type which can be performed on a portion of data stored within a memory system and a second type which can be performed on the same portion of data...." as recited in claim 1.

Claims 7, 13, 18, 24, 29, 34, 39, and 43 contain similar limitations as claim 1 and are patentable for at least similar reasons.

All dependent claims are patentable for at least the same reasons as the claims on which they depend.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Enclosed is a $50 check for excess claim fees. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 11/9/2006

Whitney A. Fellberg
Reg. No. 59,173

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906